[ACTIVE PATH EXTRACTION FOR HDL CODE]

Abstract of Disclosure

Start and stop signals are obtained from a user, with associated start and stop times, as well as circuit simulation results. The simulation results are utilized to determine which of the components in the circuit are active components, which are any components that have an active output signal.Active output signals obtain a state between the start and stop times in response to a state change of the start signal. The user output equipment is utilized to provide the active components and the active output signals to the user. Signal activity is presented in a graphical form that shows the active path circuit, and active value changes that cause output signals to become active. The user may select time values at which signals become active to see in a graphical manner the propagation of a start signal state change through the circuit.

Figures